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APPLICATION

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TITLE: PLATING A CONDUCTIVE MATERIAL ON A DIELECTRIC MATERIAL

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PLATING A CONDUCTIVE MATERIAL ON A DIELECTRIC MATERIAL

Background

This invention relates generally to processes for manufacturing semiconductor integrated circuits.

Copper seed layers are generally deposited on Cu diffusion barrier materials to enable those materials to receive copper electroplating. However, as silicon processes move to ever smaller features, the ability to deposit copper seed layers, for example using physical vapor deposition techniques, with minimal overhang and asymmetry, adequate sidewall coverage and a sufficient field thickness for gap fill is increasingly in doubt.

Physical vapor deposition of barrier materials has associated overhang, asymmetry, and sidewall coverage issues prior to copper electroplating. Physical vapor deposition of copper seed layers may further reduce the plating budget within a given feature. Alternatively, a wafer may be immersed in a palladium solution to chemically activate the surface prior to electroless plating of a copper or a copper diffusion barrier. However, this involves an additional chemical expense, process step and bath recycle requirements prior to electroless barrier deposition.

In general there is a need for better ways to form materials on dielectric materials.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view at an early stage of fabrication in accordance with one embodiment of the present invention;

Figure 2 is an enlarged cross-sectional view of the structure shown in Figure 1 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 3 is an enlarged cross-sectional view of the embodiment shown in Figure 2 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 4 is an enlarged cross-sectional view of the structure shown in Figure 3 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 5 is an enlarged cross-sectional view at a subsequent stage of the structure shown in Figure 4 in accordance with another embodiment of the present invention;

Figure 6 is an enlarged cross-sectional view illustrating one embodiment for forming the structure shown in Figure 4;

Figure 7 is an enlarged cross-sectional view of the embodiment shown in Figure 6 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 8 is an enlarged cross-sectional view of the structure shown in Figure 7 at a subsequent stage in accordance with one embodiment of the present invention; and

Figure 9 is an enlarged, schematic, cross-sectional view of the structure shown in Figure 8 at a subsequent stage in accordance with one embodiment of the present invention.

Detailed Description

In accordance with various embodiments of the present invention, a semiconductor wafer may include a semiconductor substrate having a dielectric material 12, such as an interlevel dielectric (ILD), formed thereon as shown in Figure 1. The material 12 may be an ultra low dielectric constant material, such as carbon doped oxide (CDO), or the material may be a sacrificial dielectric, as another example. The material 12 may be exposed on an upper surface. Also exposed thereon is a disparate material 14, such as a metal material. The material 14 may be a copper filled trench in one embodiment. A copper or other metal shunt 16 may be formed over the material 14 in one embodiment.

A second level interlayer dielectric material 18 may then be deposited over the layer 12, for example in accordance with the well known damascene process as shown in Figure 2. Of course, the techniques described herein

can be applied to any layer of a multi-layer structure. Again, the material 18 may be an ultra low dielectric constant dielectric material or a sacrificial dielectric, as two examples.

Referring to Figure 3, using trench and via techniques including lithography, etching, and cleaning, a T-shaped trench 20 may be formed in the material 18 as shown in Figure 3 in one embodiment. As shown in Figure 4, a conductive polymer 22 may be selectively deposited on the exposed surfaces of the dielectric 18 while avoiding deposition on the exposed surface of a shunt 16 made of a disparate material such as a metal. One technique for forming the selective deposition of a conductive polymer is described in greater detail in connection with Figures 6 through 9.

Once the conductive polymer layer 22 has been defined, an electroless deposition step may be achieved to form the layer 24 as shown in Figure 5. In the case of a dielectric 18 that is capable of acting as a diffusion barrier, the material 24 may be copper or other metal that is deposited by electroless deposition. In the case where the material 18 is not a sufficient diffusion barrier, a copper diffusion barrier, such as electroless cobalt boron phosphorous, may be formed as the layer 24 to act as a diffusion barrier. Thereafter, in the case where the layer

24 is a diffusion barrier, a copper or other metal layer may be deposited over the layer 24.

Through surface grafting, a conductive polymer 22 may be caused to attach to a material with abstractable hydrogen. The materials with abstractable hydrogen may be known as proton donors and examples include organic materials or materials with organic moieties. Dielectric materials, such as the material 18, may commonly have abstractable hydrogen. Conversely, materials, such as a metal, have no such abstractable hydrogen and, therefore, will not be subject to induced photografting or polymerization.

As a result, the polymerization can be caused to occur selectively on the surface where abstractable hydrogen is available such as the dielectric 18. In regions without such abstractable hydrogen, such as where the shunt 16 is exposed, no such polymerization will occur. The polymer may be formed selectively on a surface in some regions and not in others. In some embodiments this may avoid unnecessary photo etching and masking steps, decreasing the cost of the semiconductor processing.

A variety of techniques may be utilized to induce surface grafting and polymerization. For example, photo induced graft polymerization may be achieved using benzophenone moieties. Other examples include radical photopolymerization, hydrogen abstraction on organic

surfaces with molecules other than benzophenone, cationic and anionic polymerizations, and azide functionalization, to mention a few examples. In general, it is desirable to induce polymerization on regions that are polymerizable while avoiding polymerization on regions, such as metals, that are not polymerizable.

In accordance with one embodiment of the present invention, photo induced graft polymerization may be implemented using benzophenone to form the conductive polymer layer 22 only over the dielectric 18 and not over the metal shunt 16. Referring to Figure 6, the dielectric material 18, that has abstactable hydrogen, may have a surface chemistry including hydrogen (H) moieties 26, and organic molecules (e.g., R1), in any of a variety of forms. The material 18 may be coated with a solution of benzophenone and irradiated using ultraviolet radiation at 340 nanometers (nm), in accordance with one embodiment of the present invention. Other wavelengths may also be used such as 365nm.

Ultraviolet radiation breaks down the double bond between the carbon and the oxygen forming a benzophenone derivative reactable with a variety of other organic moieties. Thus, as shown in Figure 7, as a result of the breakdown of the benzophenone solution, ketal moieties 28 may be attached in place of some of the hydrogen moieties 26 previously present on the surface of the material 18.

Advantageously, the benzophenone solution is provided in a solvent with poor proton donor activity such as benzene. In addition, the solvent is advantageously transparent at the illumination intensities that are utilized.

Of course, the metal shunt 16 surface does not react with the benzophenone via the ultraviolet induced hydrogen abstraction mechanism. Only the organic materials or materials with an abstractable hydrogen are functionalized. The wafer may then be washed with an appropriate rinse solution, such as acetone or methanol, to mention a few examples, to remove excess benzophenone.

Next, as shown in Figures 8 and 9, a coating material that is susceptible to free radical polymerization is coated over the wafer and the wafer is, again, exposed to ultraviolet light. The free radical benzophenone ketal moieties 28 then serve as a surface photoinitiator, causing *in situ* polymerization of the coating material. The coating material that is polymerized to form the conductive polymer 22 may be an oligomer end-functionalized with vinyl groups. The oligomer chains may be chosen such that they are conductive enough to act as a seed layer for electroplating or such that they contain moieties that activate electroless deposition of a diffusion barrier, such as a copper diffusion barrier. Examples of conductive oligomers that lead to an activating polymer include

polyaniline, polypyrrole, polythiophenes, polyethylenedioxythiophene, and poly(p-phenylene vinylene)s. An example of a monomer for electroless activation includes sigma-4-styrene bis(triphenylphosphine) palladium chloride.

Polymer materials, such as benzocyclobutene, certain polyimides, NH_3 post-treated hydrogen silsesquioxane, and carbon doped oxide provide significant resistance to copper diffusion/migration and, therefore, may serve as barriers to copper diffusion. The barrier properties of the dielectric material 18 may be improved by further cross-linking. Electroless plating of barrier material layers may be used if the polymer contains sites that will activate the process. For example, palladium activates CoBP electroless deposition. Copper electroplating directly onto CoBP is well known and does not require a physical vapor deposition copper seed layer. Modification of the dielectric surface to enable electroless plating may be achieved by plasma pretreatment (see M. Charbonnier, M. Alami, and M. Romand, J. Electro. Soc., 143, 472 (1996)), and UV Induced Graft polymerization of Argon plasma-pretreated poly (tetrafluoroethylene) (PTFE) surfaces to improve adhesion (see G.H. Yang, E.T. Kang, and K.G. Neoh, Appl. Surf. Sci., 178, 165 (2001)), as well as simple wafer immersion into $PdCl_2$ bath to catalyze the dielectric surface prior to electroless deposition, (see S. Shingubara, T.

Ida, H. Sawa, H. Sakaue, and T. Takahagi, Adv. Metallization Conf. Proc., p. 229 (2000)).

A solvent rinse after exposure removes any unreacted coating material. The conductive polymer 22 is selectively grown on the material 18 as shown in Figure 9. Figure 9 shows a nonexistent gap between the polymer 22 and the dielectric 18 solely for illustration purposes.

In general, a compound having a double bond that is susceptible to polymerization, such as free radical polymerization, as an example, may be utilized to form the conductive polymer 22 and to replace the ketal moieties 28 shown in Figure 8.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: